B.Sc – 2nd Semester

Paper --- Semiconductor devices (1)

UNIT – II

TRANSISTORS

Junction Transistor :– The transistor was invented in 1948 by John Bardeen, Walter Brattain and William Shockly at Bell Lab in America.

A transistor is basically a Silicon or germanium crystal containing three seperate regions. It is formed by sandwiching either a P type or n type between a pair of n or P type respectively. Accordingly there are two types of transistors

1) npn transistor 2) PnP transistor.

1) npn transistor :– A npn transistor is formed by sandwiching a thin layer of p type s/c between two n-type s/c.

(ii) Pnp transistor :– A pnp transistor is formed by sandwiching a thin layer of n type s/c between two p-type semiconductors.

Both types of transistors have three regions discussed below.

(I) Emmiter (II) Base (III) Collector

(I) Emmiter :– Emmiter is always highly doped since the function of emmiter is to emit or inject electrons (holes in case of PNP) into the base region.

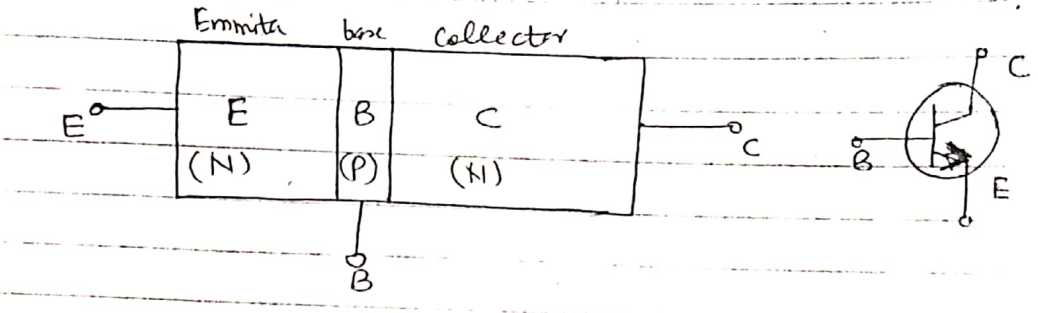
(II) Base :– Middle region is called base and is lightly doped and is very thin, so that there are less chances of recombination of carriers from emmiter and base.

(III) Collector :– Collector region is made Physically larger than the emmiter region. Since it is required to dissipate more heat. Although the two outer regions of transistor i.e emmiter and collector are of same type either n or p but their functions cannot be interchanged.

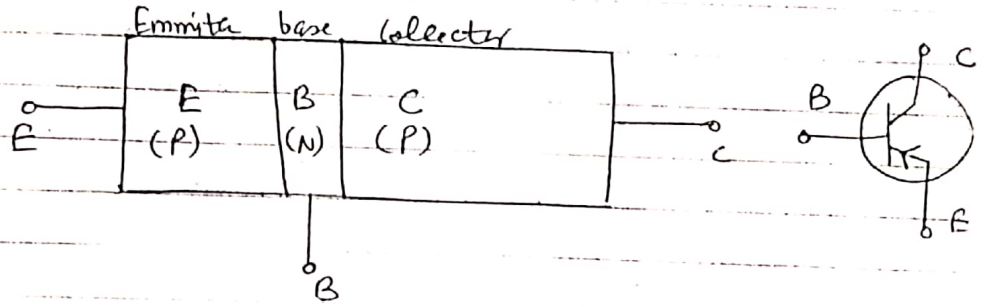
The collector has the job of collecting or gathering carriers from the base

~~The collector is moderately doped.~~

A transistor has two P-N junctions. One junction is between emmitter and base and is called emmitter base junction. The other junction is between base and collector and is called collector base junction.



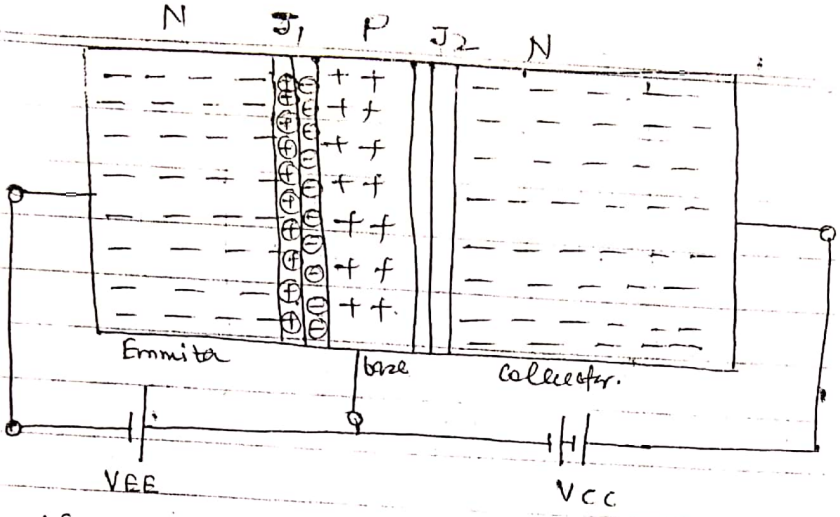
(NPN transistor)



(PNP transistor)

Both types PNP & NPN transistors are called as BJT ie bipolar junction transistor, because these are operated by two types of charge carriers (bi = two, Polar = Polarity) ie electrons and holes.

Working of NPN transistor → Let us consider a NPN transistor in which emmitter base junction is forward biased by emmitter battery V_{EE} and collector base junction is reverse biased by battery V_{CC}.

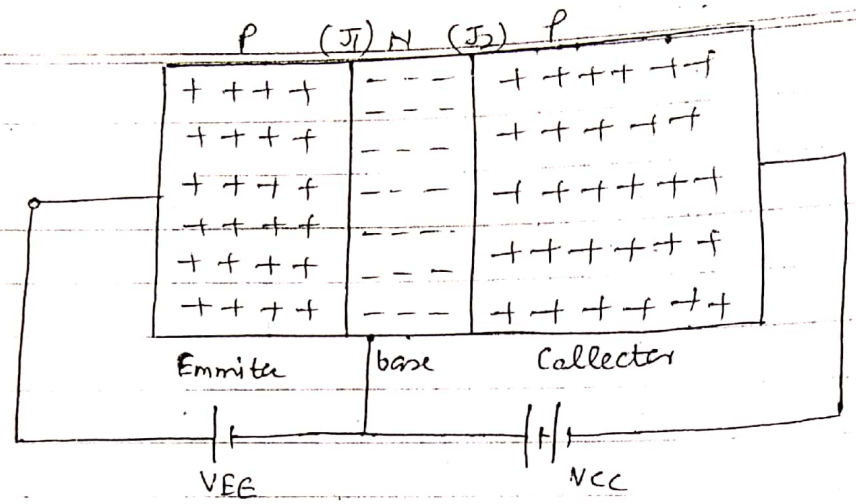


Since the emmiter base junction is forward biased, the barrier potential is reduced and depletion layer becomes narrow at jun. J1. Majority carriers i.e electrons in emmiter diffuses towards base region. Once the electrons are injected by emmiter into base, there are chances of recombination of these electrons with holes of base region. Since the base is thin and lightly doped, so the electrons of emmiter has very less chances of recombination. Only a few electrons may recombine with holes. The ratio of no. of electrons arriving at the collector to the no. of emmited electrons is called as base transportation factor. So 95% of electrons emmited by emmiter reaches the collector.

So

$$I_E = I_B + I_C$$

Working of PNP transistor → Let us consider a PNP transistor, in which emmiter base junction is forward biased by battery V_{EE} and collector base junction is reverse biased by battery V_{cc}. Fig below shows PNP transistor biased with batteries V_{EE} & V_{cc}.



The holes in the emmiter and electrons in the base are repelled towards the emmiter base junction J_1 by battery V_{EE}. After being injected into base region, the holes have a tedency to recombine with electrons in n-type base region. Since the width of base region is extremely thin and is lightly doped, so only approximately five % of holes recombines with electrons in the base region, which result in small base current. While remaining 95 % of holes reaches the collector junction. As each hole reaches the collector electrode, an electron from -ve battery terminal neutralises it. For each such recombination, a covalent bond near emmiter is broken and an electron hole pair is produced. The electron enters the terminal of battery V_{EE} and hole drifts towards collector.

It should be noted that

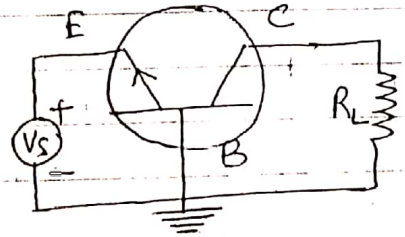
$$I_E = I_B + I_C$$

Transistor Configurations :—▷

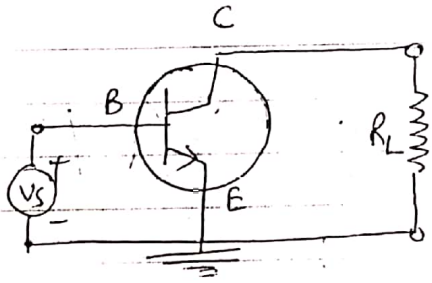
A transistor can be operated in three configurations

(i) Common base configuration
(ii) Common Emmiter configuration
(iii) Common Collector configuration

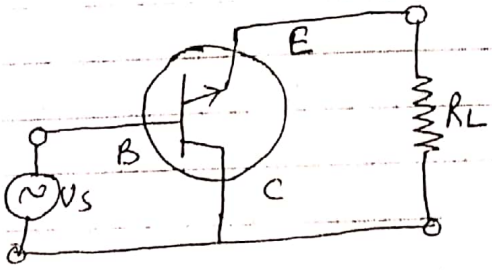
In all the three configurations, emmiter base junction is forward biased and collector base junction is reverse biased; so that transistor operates in active region



(CB)



(CE)



(CC)

A transistor behaves differently in different configurations. Out of these three configurations, the Common Collector configuration has maximum I/P resistance, but its voltage gain is less than unity.
However CE configuration is widely used because its current and voltage gain both are high.

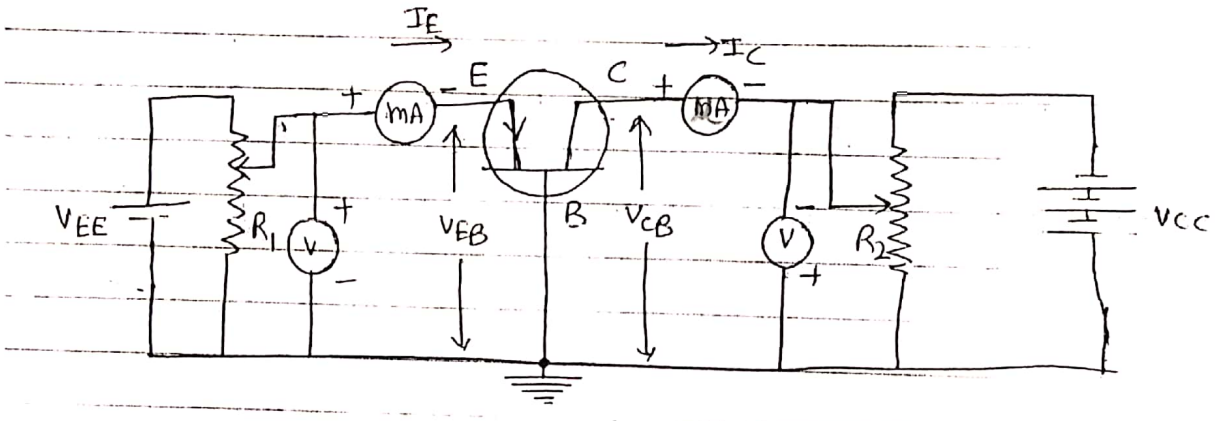
Transistor Characteristics curves:→

The Characteristic curve of transistor may be drawn in three configurations.

(i) Common base configuration characteristics.
(ii) Common emmiter Characteristics
(iii) Common collector ".

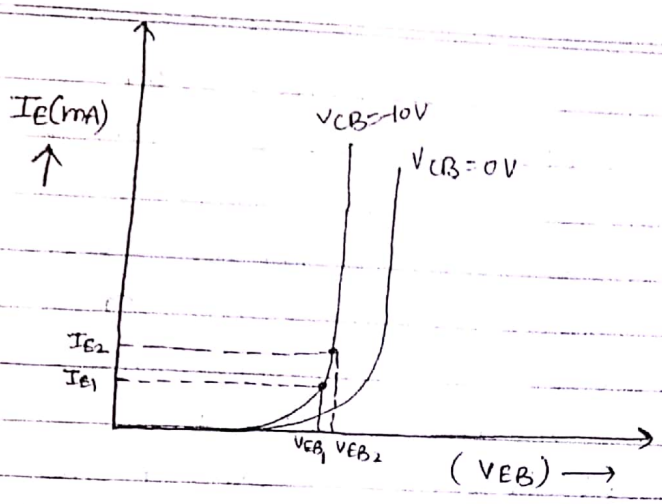
(I) Common base Characteristics:→ fig. below shows

PNP transistor connected in CB configuration.



The emmiter to base voltage V_{EB} can be varied with pottentiometer R_1 and I_E can be measured with miliammeter. Similarly collector to base voltage V_{CB} can be varied with pottentiometer R_2 and I_C can be measured with miliammeter

(i) Input Characteristics:→ To draw input cha, output voltage i.e collector to base voltage V_{CB} is kept constant and V_{EB} is varied and I_E is noted. So a curve drawn between V_{EB} and I_E for fixed value of V_{CB} is called Input Cha. Curve for CB Configuration. Fig below shows Input Cha. Curve for CB Configuration

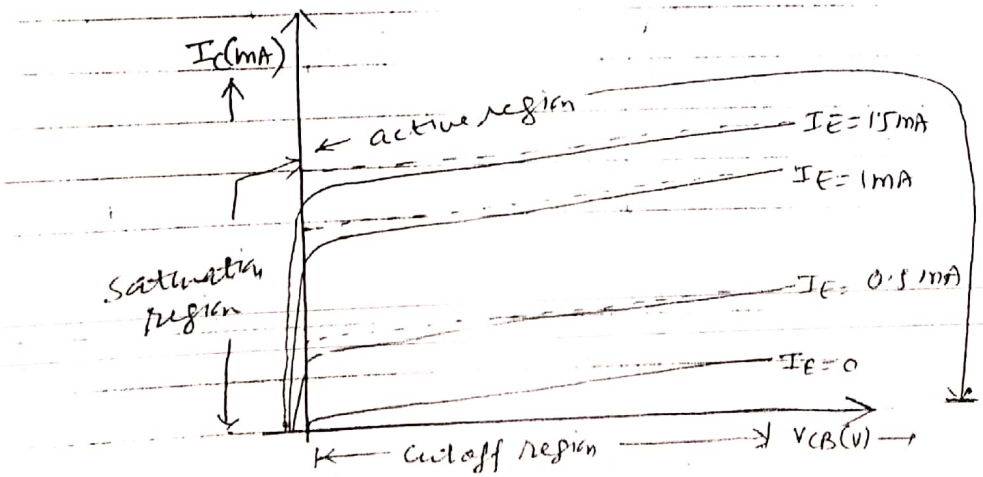


For a given value of VCB, curve is just like diode cha in forward bias region. So emmitter base acts as a diode which is forward biased.

The dynamic input resistance ri is given by

$$r_i = \frac{V_{EB_2} - V_{EB_1}}{I_{E_2} - I_{E_1}} = \frac{\Delta V_{EB}}{\Delta I_E}\Big|_{V_{CB}=\text{constant}}$$

(ii) Output Characteristics → To draw output cha, emmitter current I_E is kept constant and a curve is drawn between collector to base voltage V_{CB} and collector current I_C. Fig. below shows output cha. curve for CB configuration.



Following points are clear from the o/p Cha.

(i) The collector current I_C is approximately equal to emmiter current I_E.

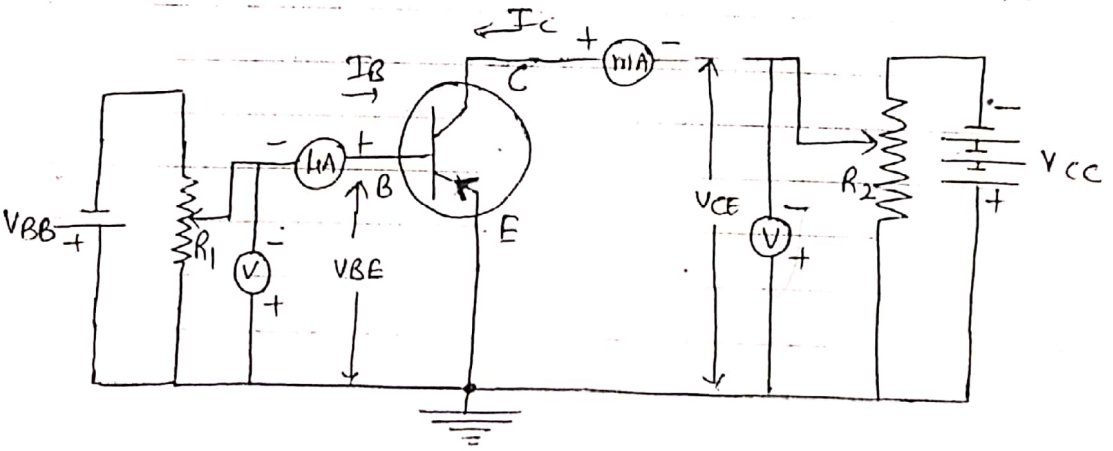
(ii) As V_{CB} becames +ve, CB junction becames FB, Hence it is called satuation Region.

(iii) Collecter current $I_C \neq 0$, when $I_E = 0$, it has a very small value called I_{CBO}, which means current between collecter and base when emmiter is open. It is basically reverse saturation current.

(iv) The dynamic o/p resistance r_o is

$$r_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{Constant}}$$

(II) Common Emmiter Characteristics' → Fig below shows the PNP transistor connected in CE Configuration.

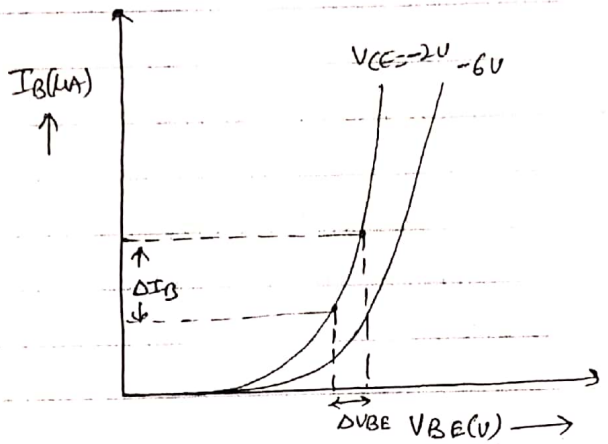


The base to emmita voltage is supplied by battery V_{BB} and it can be varied by potentiometer R_1.

Base current I_B can measured by micro ammeter.

The collecter emmitter junction is reverse biased by battery V_{cc} and V_{CE} can be varied by R_2.

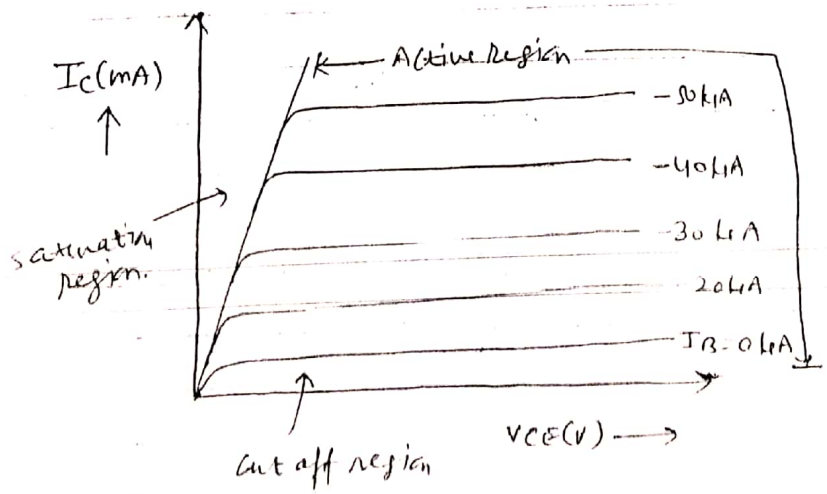
(i) Input Characteristics :→ To draw Input Cha, output is kept constant i.e V_{CE} is kept constant and V_{BE} is varied and I_B is noted. The curve drawn between V_{BE} and I_B for different values of V_{CE} is called Input Characteristic.



The dynamic Input Resistance r_i is given by

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$

(ii) Output Characteristics :→ To draw output Cha, Input current i.e base current I_B is kept constant and a curve is drawn between V_{CE} and I_C.



Following Points becomes evident from these o/p Cha. Curves.

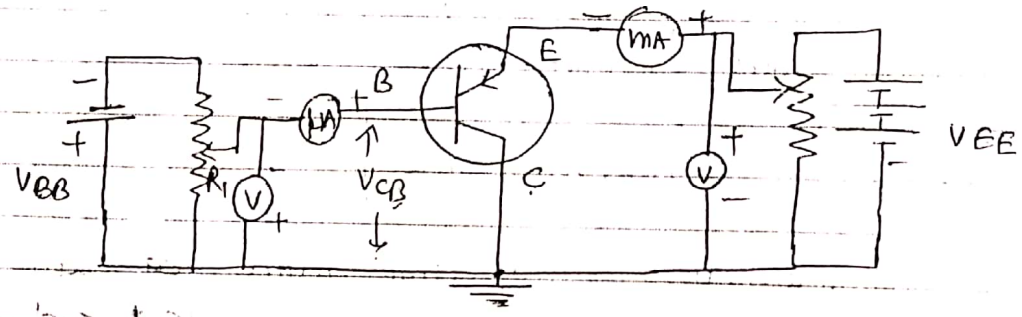
(i) In active region, I_C (collector current) increases slowly as V_{CE} increases.

(ii) The collector current is not zero, when $I_B = 0$. It has a value of I_{CEO} i.e current between collector and emitter, when base is open.

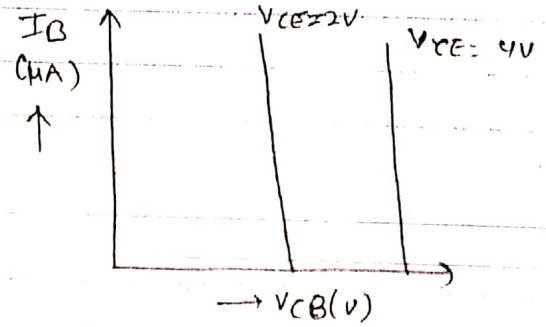
(iii) The dynamic o/p resistance is r_o given by,

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}$$

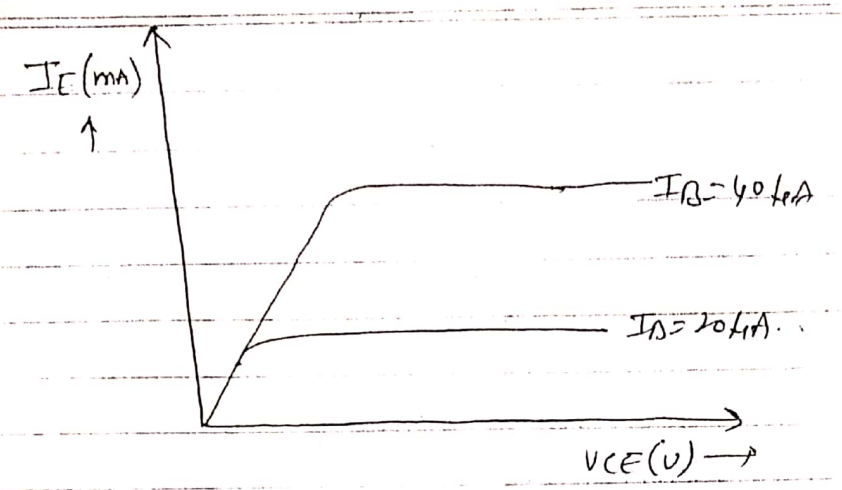
Common Collector Characteristics:— Fig below shows PNP transistor connected in common collector configuration.



(i) Input characteristics:— These are the cha. drawn between V_{CB} and I_B with V_{CE} constant.



(ii) Output characteristics:— These are the curve drawn between V_{CE} and I_E with I_B constant.



Constants of a transistor →

There are mainly two constants of a transistor dc current gain and AC current gain.

(I) In Common base configuration dc current gain i.e α_{dc} is ratio of output collector current I_C to input emmiter current I_E at V_{CB} = constant.

$$\alpha_{dc} = \left.\frac{I_C}{I_E}\right|_{V_{CB}=\text{constant}} \quad < 1$$

and AC current gain α_{ac} is ratio of ~~Small change~~ in collector current ΔI_C to Small Change in emmiter current (ΔI_E). i.e

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

(II) In Common emmiter configuration, dc current gain i.e β_{dc} is ratio of I_C and I_B at constant V_{CE}

$$\beta_{dc} = \left.\frac{I_C}{I_B}\right|_{V_{CE}=\text{constant}} \quad > 1$$

and AC current gain $\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$

Relation between α and β :—▷

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{—— (I)}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{—— (II)}$$

Where α, β are a.c current gain of CB and CE Configuration respectively.

Also

$$I_E = I_B + I_C \quad \text{—— (III)}$$

$$\Rightarrow \Delta I_E = \Delta I_B + \Delta I_C$$

$$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$$

$$\Rightarrow \frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C} - 1 \quad \text{—— (IV)}$$

from I, II and IV

$$\Rightarrow \frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Advantages and disadvantages of CE Configuration :—▷

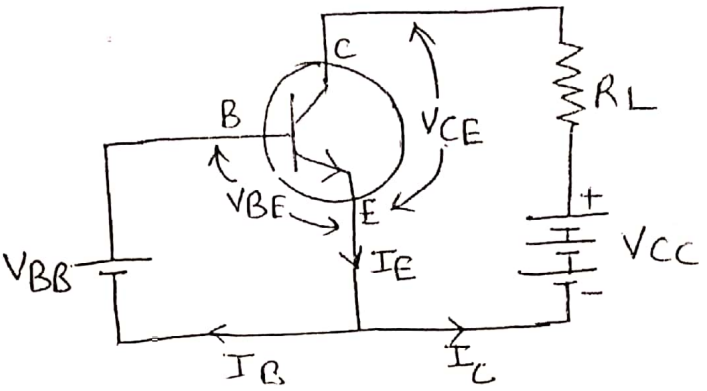
The amplifier must have high I/P resistance and low output resistance. The transistor in CE Configuration have high I/P and low O/P resistance. Moreover current gain and voltage gain of transistor in CE Configuration is very high and thus the power gain.

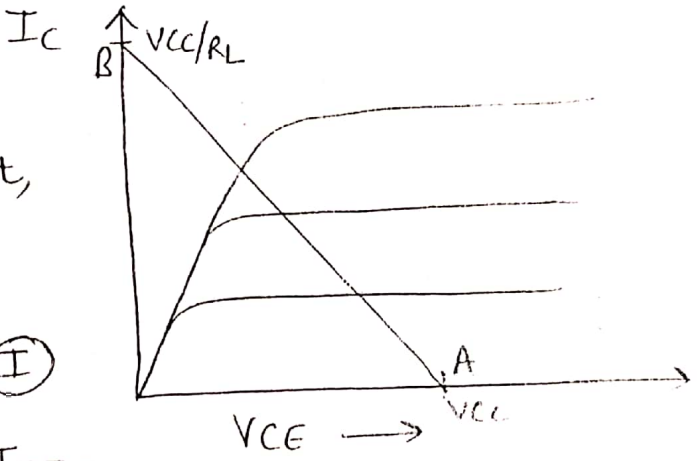
However transistor in CE Configuration gives output signal 180° out of phase with the I/P signal.

— x — x — x —

Dc load line' →

To understand the concept of dc load line, let us consider common emmiter circuit and cha. of transistor in common emmiter mode.





(DC load line)

In this circuit using KVL in output circuit,

$-V_{CC} + I_C R_L + V_{CE} = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C R_L$ — (I)

When collector current $I_C = 0$,

$\boxed{V_{CE} = V_{CC}}$

This is point A on X axis

When $V_{CE} = 0$

$\boxed{I_C = V_{CC}/R_L}$

This gives point B on y axis.

By joining these two points, we get a line called dc load line.

Biasing of Transistor :→

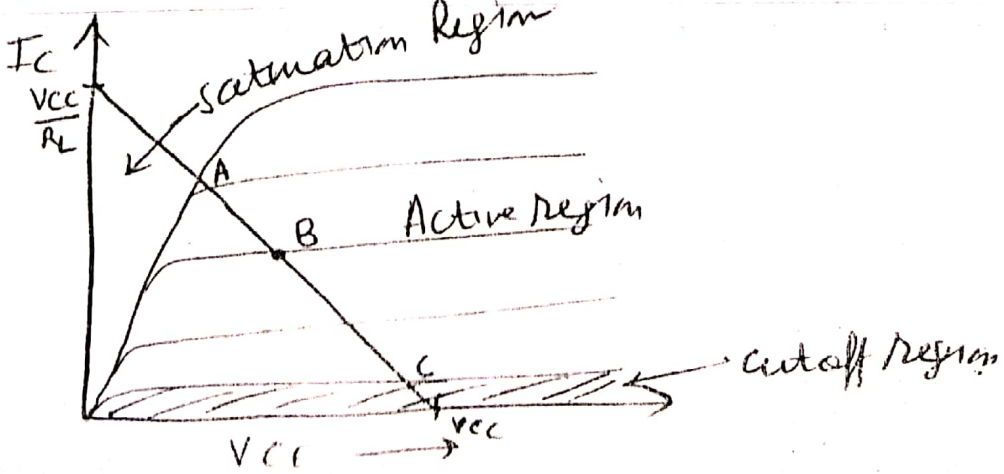
The purpose of dc biasing of a transistor is to obtain certain dc collector current at certain dc collector voltage. These fixed values of current and voltage are expressed in terms of an operating point called quiescent point. Different circuits which are used to obtain this point are called biasing circuits. Different biasing circuits used are basically providing us a stable operating point.

A transistor can have four biasing modes :-

EB Jun.	CB Jun.	operating Mode
Forward biased	forward biased	saturation
Forward biased	Reverse biased	Active
Reverse biased	Reverse biased	cut off
Reverse biased	forward biased	Inverse

Selection of operating point :→

For proper working of transistor as an amplifier, oscillator etc, the operating point must be chosen with care. The operating point lies on the load line. To see which operating point is right, let us consider transistor CE cho. and a dc load line drawn on it.



When static conditions are setup in transistor circuit, an a.c signal voltage is applied to input circuit. Due to this signal, changes in base current and hence collector current takes place with time. Fig① below shows variation in base current, variations in collector current and variations in V_{CE}, if operating point is chosen at point A, i.e near to saturation region.

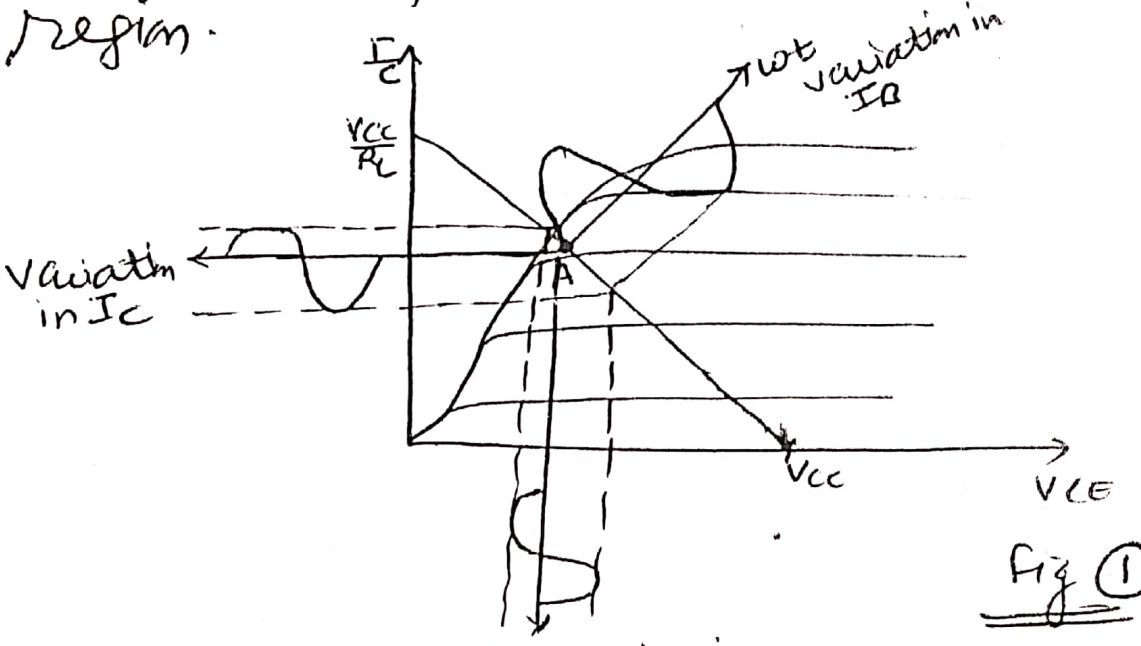


Fig ①

If operating point is at A, part of output current and voltage is cut off at the five half of base current cycle. So A is not a suitable operating point.

If operating point is chosen at B i.e in mid of active region, there will be no distortion in output and hence B is a suitable operating point. This is shown in fig ②.

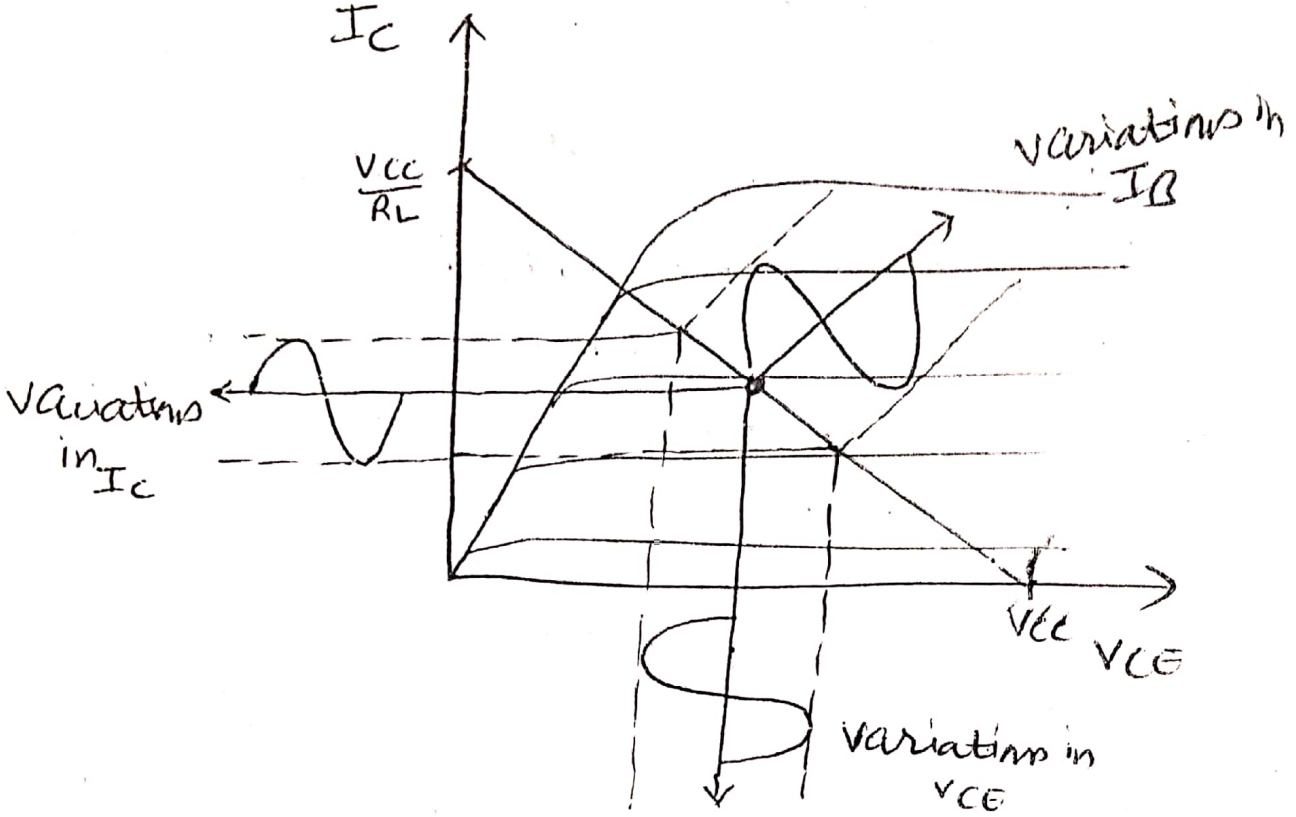


fig (2)

If operating point is chosen at point c i.e. near to cut off region, then output signal is distorted. Hence it is not a suitable operating point as shown in fig (3) below

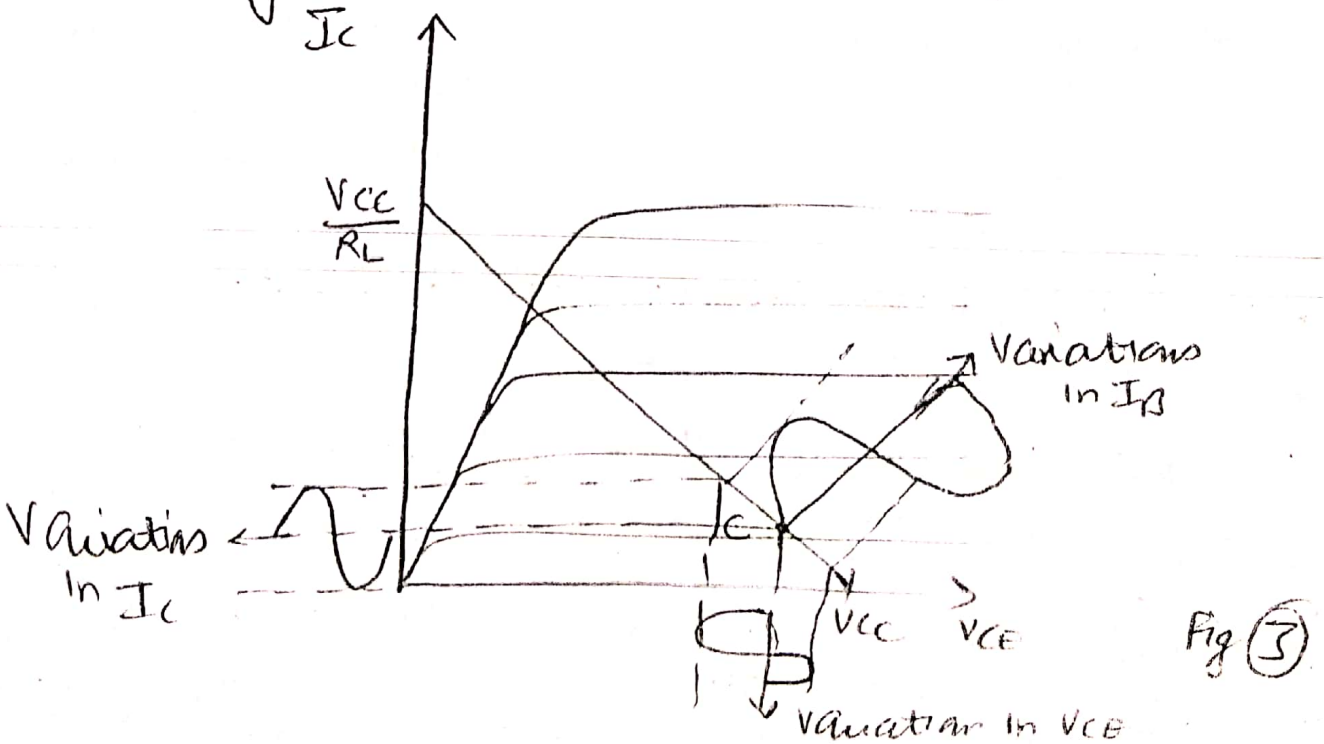


Fig (3)

Bias stabilization! →

Bias stabilization means that the operating point should remain at the fixed position and may not change with the use of circuit due to any cause.

There can be following reasons for the shift of operating point! →

(1) The transistors parameters change with the change in temperature. The flow of current in collector circuit produces heat at collector junction. This increases the temperature and thus resulting in breaking of covalent bonds in this region. This will increase leakage current I_{CO} and hence there will be increase in collector current I_C in the circuit. given by,

$$I_C = \beta I_B + I_{CO}$$

With this increase in I_C, temp will further increase and process is repeated. Ultimately I_C will saturate and transistor operating point will shift in saturation region.

(2) The current gain β changes from one ckt to other, hence changes the operating point.

Requirement for proper biasing! →

For proper biasing of transistor circuit, following points should be kept in mind -

(1) The operating point should be selected in middle of active region.

(ii) The collector current should not change with temperature variations.

(iii) The operating point should be made independent of transistor parameters, so that it may not shift, of transistor is replaced by another transistor of same type in circuit.

Types of Biasing Circuits :→

following biasing circuits are widely used to operate the transistor in Active region, cut off or saturation region.

(i) Fixed bias circuit

(ii) Collector to base bias circuit

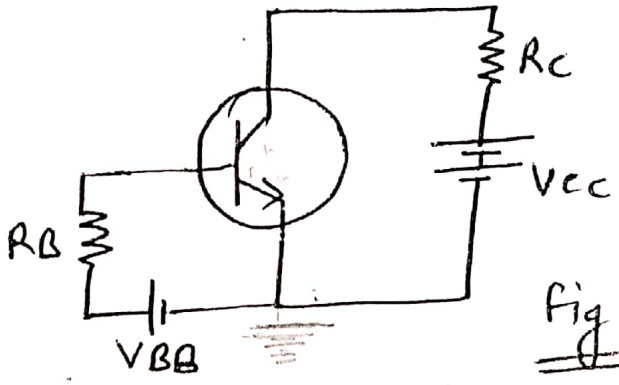
(iii) Bias circuit with Emmiter Resistance

(iv) Voltage divider biasing ckt

(v) Emmiter bias circuit

Fixed bias circuit →

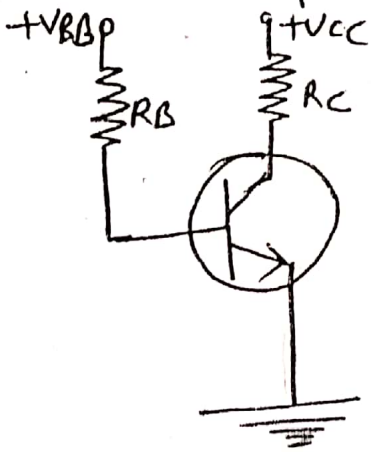
Fig 1 below shows a fixed bias circuit. In this circuit emmiter base junction is forward biased by battery V_{BB} and collector emmiter junction is reverse biased by battery V_{CC}. R_B resistance drops major portion of voltage across it.



(Fixed bias ckt)

Fig 1.

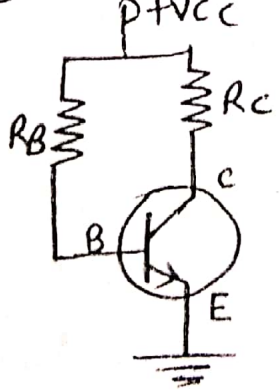
Fig 1 can also be represented as fig 2 shown below



(fixed bias ckt)

Fig 2

In actual practice, only one battery is used as shown in fig 3.



(fixed bias ckt.)

Fig 3

To Analyse fixed bias circuit, input section and output sections are seperately shown below in fig 4 and fig 5.

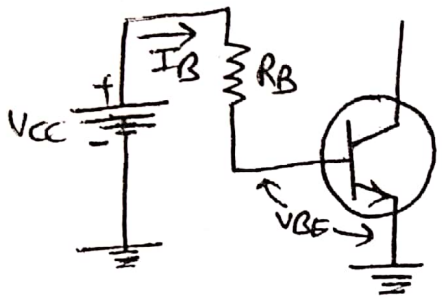


fig 4

input section of fixed bias circuit

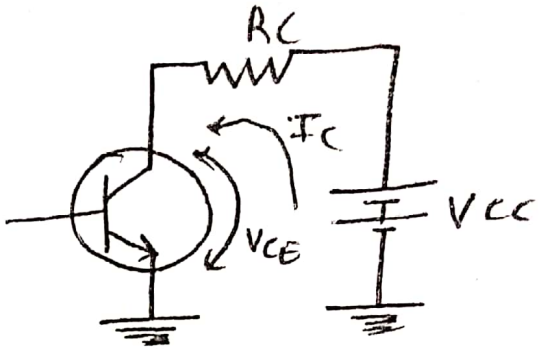


fig 5

output section of fixed bias circuit

Applying KVL to input section,

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\Rightarrow V_{CC} = I_B R_B + V_{BE} \quad \text{——— (I)}$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

($V_{BE} \approx 0.3V$ for Ge and $.7V$ for Si), so it is neglected

$$\Rightarrow I_B = \frac{V_{CC}}{R_B} \quad \text{——— (II)}$$

V_{CC} and R_B are kept fixed, so base current I_B is also fixed.

Now Applying KVL to output section,

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$\Rightarrow V_{CC} = I_C R_C + V_{CE} \quad \text{— (III)}$$

For transistor to be biased in Active region,

$$I_C R_C < V_{CC}$$

$$\Rightarrow \boxed{I_C < \frac{V_{CC}}{R_C}} \quad \text{— (IV)}$$

From (III), $V_{CE} = V_{CC} - I_C R_C$ — (V)

Hence V_{CE} remains constant as I_C is constant. because $\boxed{I_C = \beta I_B}$ and I_B is constant fixed acc. to eq (II).

So operating point (V_{CE}, I_C) is fixed.

Drawbacks of fixed bias :→

1. If transistor is replaced by another transistor current I_C changes because $I_C = \beta I_B$ and β changes due to change of transistor. Hence operating point will shift.
2. Moreover temperature change increases I_C and hence operating point is not independent of temperature.

Collector to base bias circuit :—→

In this circuit, resistance R_B is connected to collector instead of connecting it with battery V_{CC} (as in case of fixed bias ckt). Fig① below shows collector to base bias circuit.

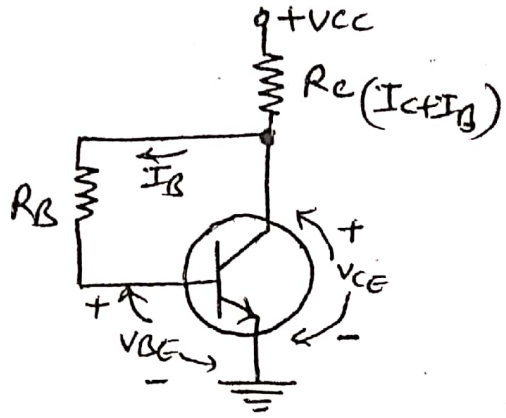


fig 1

Applying KVL in input section, —

$$-V_{BE} - I_B R_B - (I_C + I_B) R_C + V_{CC} = 0$$

$$\Rightarrow V_{CC} = I_B R_B + (I_C + I_B) R_C + V_{BE} \quad \text{—(I)}$$

$$\Rightarrow V_{CC} = I_B R_B + I_C R_C + I_B R_C + V_{BE}$$

$$\Rightarrow \frac{(V_{CC} - I_C R_C) - V_{BE}}{R_B + R_C} = I_B \quad \text{—(II)}$$

Applying KVL in output section, we get,

$$-V_{CE} - (I_B + I_C) R_C + V_{CC} = 0$$

$$\Rightarrow V_{CC} = I_B R_C + I_C R_C + V_{CE}$$

$$\Rightarrow V_{CC} \simeq I_C R_C + V_{CE} \qquad [\because I_B << I_C]$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C \quad \text{—(III)}$$

From (II) and (III), we get,

$$I_B = \frac{V_{CE} - V_{BE}}{R_B + R_C} \quad \text{— (IV)}$$

So value of base current I_B is Constant. Also Collector current I_C remains same so long as β remains same because $I_C = \beta I_B$.

Following points are found from above analysis—

(1) When temp. increase β increase. This increase I_C, So from eqn (III), we find that V_{CE} decreases. Hence from eqn (IV) I_B decreases. This reduced value of I_B again decreases I_C. So I_C does not increase Hence operating point is stabilized.

(2) If transistor in this circuit is replaced by another transistor having different β, The shift in operating point will be very small. TO show it, Put $I_C = \beta I_B$ in eqn (I)

$$V_{CC} = \beta I_B R_C + I_B(R_B + R_C) + V_{BE}$$

$$V_{CC} - V_{BE} = \beta I_B R_C + I_B R_B + I_B R_C$$

$$V_{CC} - V_{BE} = I_B[R_B + (1+\beta)R_C]$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} = \frac{V_{CE}}{R_B + \beta R_C} \quad \text{— (V)}$$

Because $V_{BE} << V_{CE}$
and β is large

$$I_C = \beta I_B = \frac{\beta V_{CE}}{R_B + \beta R_C} \quad \text{— (VI)}$$

Since β is in num. and den. of eq (VI)
So change in value of β does not affect much the value of I_C. also from eqn (III), V_{CE} is almost constant.

Drawback ⇒

Resistance R_B not only provide dc feedback but also causes a.c feedback.
Due to which, voltage gain reduces in case of an amplifier.

Bias circuit with Emmiter Resistance:—

This circuit is same as fixed bias circuit except that a resistance R_E is included in emmiter terminal. Fig (1) below shows a bias circuit with emmiter resistance.

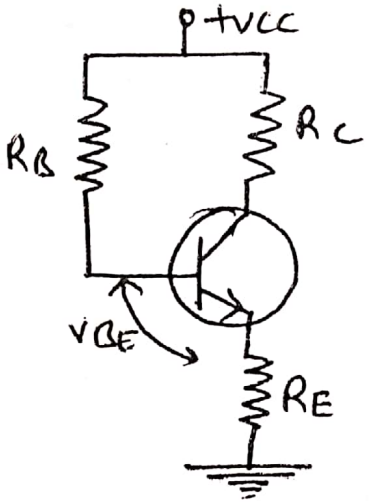


fig 1

Applying KVL to Input section, We get,

$$-I_E R_E - V_{BE} - I_B R_B + V_{CC} = 0 \quad \text{—— (I)}$$

$$\Rightarrow I_B R_B = V_{CC} - V_{BE} - I_E R_E$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_E R_E}{R_B}$$

But $V_{CC} > V_{BE}$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - I_E R_E}{R_B}} \quad \text{—— (II)}$$

As the temperature increases, reverse leakage current increases. This increases I_C and I_E. So voltage drop $R_E I_E$ across R_E increases

so from eqn (II), I_B decreases, so this decreases I_C because $I_C = \beta I_B$. Thus collector current I_C is not allowed to increase to much extent.

This circuit also provides stabilization, when transistor has to be replaced by another transistor having different value of β.

To prove this, we know that

$$I_C = \beta I_B \Rightarrow \beta = \frac{I_C}{I_B} = \frac{I_E - I_B}{I_B}$$

$$\Rightarrow \beta I_B = I_E - I_B$$

$$\Rightarrow \beta I_B + I_B = I_E \quad \text{—— (III)}$$

Put (III) in (I), we get

$$V_{CC} = R_B I_B + V_{BE} + R_E (I_B + \beta I_B)$$

$$V_{CC} = R_B I_B + V_{BE} + I_B R_E + \beta I_B R_E$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E + \beta R_E}$$

$$\Rightarrow I_B \simeq \frac{V_{CC}}{R_B + \beta R_E}$$

$$\therefore I_C = \beta I_B = \frac{\beta V_{CC}}{R_B + \beta R_E} = \frac{V_{CC}}{\frac{R_B}{\beta} + R_E} \quad \text{—— (IV)}$$

It is clear that I_C is independent of β, only if $\frac{R_B}{\beta} \ll R_E$

Voltage divider biasing circuit →

fig (1) below shows a voltage divider biasing circuit.

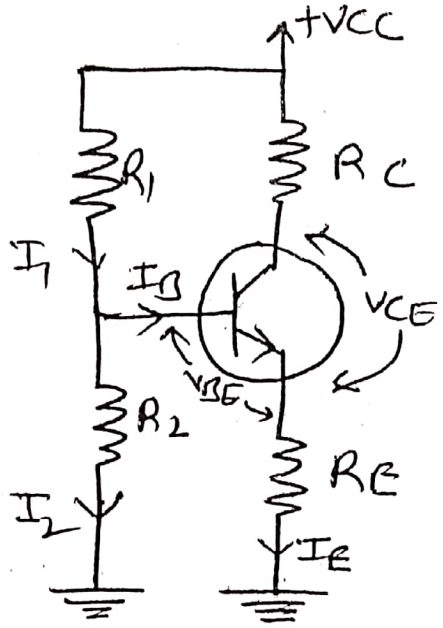


Fig 1

R_B of biasing ckt with emmiter resistance is named as R_1 and additional resistance R_2 is introduced. R_1 and R_2 forms a voltage divider. In this circuit, operating point can be made independent of β. Thats why voltage divider biasing circuit is sometimes called as biasing circuit independent of β.

To Analyse this circuit, fig 2 shows the voltage divider biasing circuit redrawn using two supply voltages.

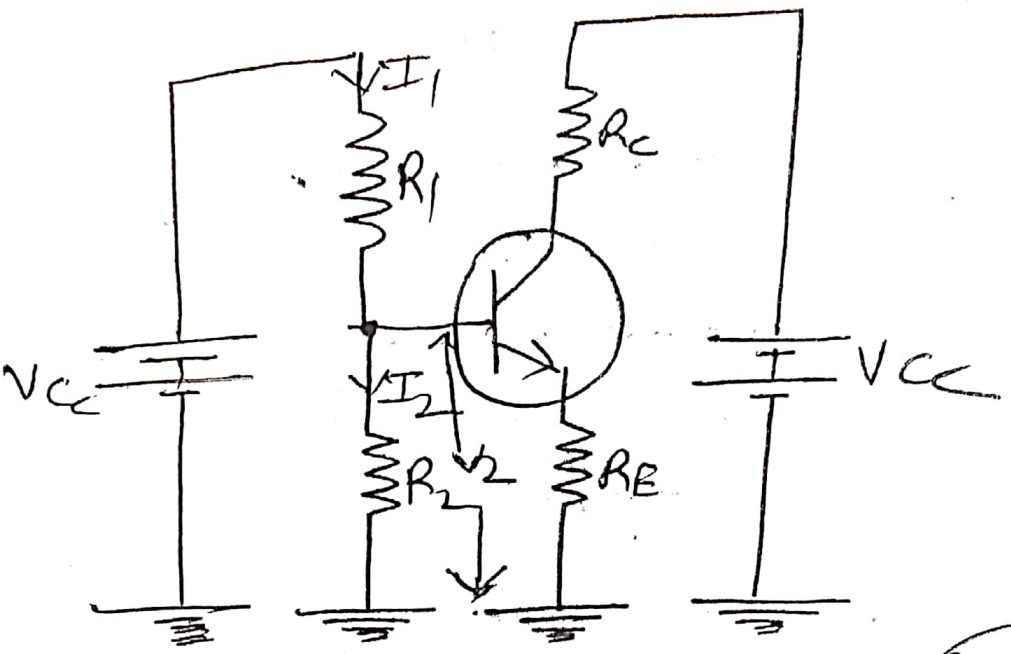


Fig 2

The resistance R_1 and R_2 are so selected that base current I_B is very small. Since I_B is small, current I_1 through R_1 flows almost through R_2.

and $I_1 = I_2 = I$ (say)

and resistance R_1 and R_2 are effectively in series.

$$\therefore V_{CC} = I(R_1 + R_2)$$

$$\Rightarrow I = \frac{V_{CC}}{R_1 + R_2} \quad \text{——— (I)}$$

$$\therefore V_2 = I R_2 \quad \text{——— (II)}$$

From (I) and (II)

$$V_2 = \frac{V_{CC} R_2}{R_1 + R_2} \quad \text{——— (III)}$$

The voltage at emitter is

$$V_E = V_2 - V_{BE} \quad \text{——(IV)}$$

Also

$$I_E = \frac{V_E}{R_E} = \frac{V_2 - V_{BE}}{R_E} \quad \text{——(V)}$$

Also $I_C \approx I_E$ ——(VI)

From output circuit,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad [\text{By KVL}]$$

$$= V_{CC} - I_C R_C - I_C R_E$$

$$V_{CE} = V_{CC} - I(R_C + R_E) \quad \text{——(VII)}$$

Clearly V_{CE} and I_C dont depend upon β. So operating point is independent of β. Due to this, if a transistor is damaged in a ckt, then it can be replaced by another transistor having diff. β.